Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L26	L25 same internal	101	L26
L25	L24 same l22	101	L25
L24	command adj1 decoder	2027	L24
L23	L22 and bist	2	L23
L22	L20 same l9	160	L22
L21	L20 same bist	1	L21
L20	L19 same l7	2814	L20
L19	$ram	1137389	L19
L18	L17 and l7	15	L18
L17	L12 same bist	128	L17
L16	L13 and bist	0	L16
L15	L13 and bist	0	L15
DB=USPT,PGPB; PLUR=YES; OP=OR			
L14	(4564926| 4802135| 5394373| 5598376| 5668773| 5854769| 5923604| 5991226)![pn]	8	L14
DB=USPT; PLUR=YES; OP=OR			
L13	L10 same l12	20	L13
L12	microprocessor	157549	L12
L11	L10 same l1	56	L11
L10	L9 same l7	368	L10
L9	external same internal	181044	L9
L8	L7 and l3	30	L8
L7	command near3 decod$	8714	L7
L6	L5 and l3	5	L6
L5	command adj1 decode	834	L5
L4	L1 same l2	18	L4
L3	L2 and l1	64	L3
L2	bist	1171	L2
L1	sdram	4086	L1

END OF SEARCH HISTORY

WEST

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L25: Entry 83 of 101 File: USPT May 4, 1999

DOCUMENT-IDENTIFIER: US 5901304 A
TITLE: Emulating quasi-synchronous DRAM with asynchronous DRAM

Detailed Description Text (7):
FIG. 5 is a block diagram of the interface conversion circuit 211. The input buffers 401 represent all the input control buffers, such as ERAS, ECAS, EWE (external write enable), ECS (external chip selection), CLK (clock), and ADD (address). All input buffers are synchronous latch circuits. The command decoder consists of a state machine 410 and combination logic 420. The state machine 410 is a gate-array-based design. The combination logic 420 can be synthesized through a hardware description language (HDL). The command decoder receives the external control signals and address from the input buffers 401, converts these signals to internal control signals 430 (i.e., IRASa, ICASa, . . . , IRASb, ICASb, . . .)and burst address generator 440 and burst control signal 441 to select the data I/O buffer circuit.

WEST

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L8: Entry 7 of 30 File: USPT Nov 26, 2002

DOCUMENT-IDENTIFIER: US 6486493 B2
TITLE: Semiconductor integrated circuit device having hierarchical test interface circuit

Brief Summary Text (13):
The DRAM core MCR is a synchronous DRAM (SDRAM) which takes in an operation mode instruction signal and receives/transmits data synchronously with a supplied clock signal.

Brief Summary Text (15):
As shown in FIG. 16, by providing the test interface circuit TIC, the DRAM core MCR is completely disconnected from the logic device (large-scale logic device LG), so that the DRAM core MCR can be directly accessed via the test pin terminal group TPG. Consequently, the DRAM core MCR can be controlled and monitored directly from the outside by a memory tester or the like. By providing the test interface circuit TIC, according to a direct memory access test, an operation test which is substantially the same as that conducted on a general DRAM (SDRAM) by using a conventional memory tester can be conducted.

Brief Summary Text (19):
The test interface circuit TIC includes a latch/command decoder 1 for performing data processes of taking in the test control signal TCMD, test address TAD, and test input data TDin supplied to the test pin terminal group TPG synchronously with the test clock signal TCLK, decoding the test control signal to an internal command (operation mode signal) so as to be issued to the DRAM core MCR, expanding the 8-bit test input data TDin to write data of 256 bits, and the like.

Brief Summary Text (20):
The test interface circuit TIC further includes: a mode register 2 for storing information such as column latency of the DRAM core MCR; a CA shifter 3 for generating a read data selection signal RD_S by shifting a read selection signal supplied from the latch/command decoder 1 in accordance with the column latency information stored in the mode register 2; and a read data selection circuit 4 for performing 256:8 test output data selection of selecting 8-bit data from 256-bit data read from the DRAM core MCR in accordance with the read data selection signal RD_S from the CA shifter 3.

Brief Summary Text (24):
FIG. 18 is a diagram more specifically showing the configuration of the latch/command decoder illustrated in FIG. 17.

Brief Summary Text (25):
Referring to FIG. 18, the latch/command decoder 1 includes: a latch circuit 1a for taking in and latching the test control signal TCMD, the test address TAD, and the test input data TDin which are supplied to the test pin terminal group TPG in response to the rising edge of the test clock signal TCLK; a command decoder 1b for receiving and decoding a predetermined bit in the test control signal TCMD and the test address TAD from the latch circuit 1a and generating a command of designating an operation mode; a bit width expanding circuit 1c for expanding the 8-bit test input data TDin from the latch circuit 1a to 256-bit write data; and a latch circuit 1d for taking in and latching output signals of the command decoder 1b and the bit width expanding circuit 1c in response to the trailing edge of the test clock signal TCLK.

Brief Summary Text (26):
A test command TIFCMD, a test interface address TIFAD, and test input data TIFDin are outputted from the latch circuit 1d and are supplied to the DRAM core MCR via the selector 5. A command from the command decoder 1b is also supplied to the mode register

2. When a mode register set mode is designated, an address bit, test data, or the like is stored into the mode register 2.

Brief Summary Text (28):
The command decoder 1b receives the test control signal TCMD and a predetermined address bit and generates an internal command for designating an operation mode, a row active command ACT, a bank precharge command PRE, a write command WRITE, a read command READ, an auto refresh command REFA, and the like.

Brief Summary Text (38):
In dock cycle #2, the test control signal TCMD indicative of writing of data is supplied from an external memory tester to the DRAM core MCR. The test control signal TCMD is decoded to the write command (operation mode instruction signal) WRITE indicative of writing of data by the latch/command decoder 1. When the write command is supplied, the test input data TDin(DA) is also simultaneously supplied to the test pin terminal group TPG. The write command WRITE and the test write data DA are also transferred synchronously with the test clock signal TCLK in the test interface circuit TIC.

Brief Summary Text (39):
In the latch/command decoder 1, the 8-bit test input data DA (TDin) is converted to the 256-bit internal write data DAin by the bit width expanding circuit 1c. That is, an 8-bit data line is expanded and developed to a 256-bit data line.

Brief Summary Text (40):
Further, the test control signal TCMD to be decoded to the read command READ for instructing reading of data is supplied from the external memory tester in clock cycle #3. In the following clock cycle #4, a test control signal to be decoded to the write command WRITE for instructing writing of data is supplied.

Brief Summary Text (43):
By providing the test interface circuit TIC as described above, the DRAM core MCR can be directly accessed from an external memory tester, so that the direct memory access test can be conducted. The operation test necessary for the DRAM core MCR provided in the system LSI can be therefore conducted by using a general SDRAM memory tester.

Drawing Description Text (19):
FIG. 18 is a block diagram more specifically showing the configuration of a latch/command decoder illustrated in FIG. 17; and

Detailed Description Text (38):
In the DRAM core MCR1, a sub block is selected from the eight sub blocks in accordance with the upper three bits RA<11:9> in the row address. Consequently, the uppermost address bit TAD<12> in the test address TAD<12:0> is latched into the latch/command decoder 1 in the test interface circuit TIC1 for a row active period. The lower 12 bits RA<11:0> are transmitted as a row address to the DRAM core MCR1.

Detailed Description Text (39):
In the case where the test control signal TCMD to be decoded to the write command WRITE for instructing writing of data is supplied to the DRAM core MCR1, when the address bit TAD<12> latched in the latch/command decoder 1 is "1", the write command WRITE is converted to a no-operation command NOP and the no-operation command NOP is transmitted to the DRAM core MCR1. In the case where the test control signal TCMD to be decoded into the read command READ for instructing reading of data is supplied, the read command READ is issued as it is to the DRAM core MCR1. It is sufficient to execute such a control by the latch/command decoder 1 in the test interface circuit TIC1.

Detailed Description Text (40):
In the DRAM core MCR2, a sub block is selected from the four sub blocks in accordance with the upper two bits RA<10:9> of the row address. Consequently, the thirteenth and twelfth upper bits TAD<12:11> in the test address TAD<12:0> are latched into the latch/command decoder 1 during the row active period, and the lower 11 bits RA<10:0> are transmitted as a row address to the DRAM core MCR2. In the case where the test control signal TCMD to be decoded to the write command WRITE is supplied, when the latched test address TAD<12:11> of two bits is described as TAD<12> and TAD<11> and TAD<12:11>=(1, 1), (1, 0), or (0, 1), the latch/command decoder 1 included in the test interface circuit TIC2 converts the write command WRITE to the no-operation command NOP, and outputs the no-operation command NOP to the DRAM core MCR2. On the other hand, when the test control signal TCMD to be decoded to the read command READ is supplied,

the latch/command decoder 1 transmits the read command READ as it is to the DRAM core MCR2. It is sufficient to execute such a control by the latch/command decoder 1 in the test interface circuit TIC2.

Detailed Description Text (144):
Referring to FIG. 15, the semiconductor integrated circuit device 101 is obtained by adding a self test circuit STC for generating the test control signal TCMD, test address TAD, and the like to the semiconductor integrated circuit device 100 illustrated in FIG. 1. In the semiconductor integrated circuit device 101, the test control signal TCMD, test address TAD, and the like are not supplied from the outside via the test pin terminal group TPG but are executed by the self test circuit STC on the basis of a BIST (Built In Self Test).

Detailed Description Text (146):
With such a configuration, the single self test circuit is shared by the plurality of DRAM cores and the operation test based on the BIST function can be conducted. Any of the configurations described in the first to third embodiments can be applied as the configuration at the post stage of the upper test interface circuit TICU.

WEST

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L8: Entry 11 of 30 File: USPT Aug 20, 2002

DOCUMENT-IDENTIFIER: US 6438667 B1
TITLE: Semiconductor memory and memory system

Abstract Text (1):
When a test instruction signal is outputted from a command decoder, a test mode decoder receives the test instruction signal and outputs a test signal. When a DQM switch circuit receives the test signal, the DQM switch circuit outputs a mask/disable signal (MASK0 or MASK1) inputted to any one of two mask/disable terminals (DQML, DQMU) as a mask/disable signal inputted from the two terminals DQML and DQMU to a write amplifier/sense buffer. Therefore, it is possible to execute a mask/disable operation for all of input and output data with one of the two mask/disable terminals.

Brief Summary Text (6):
A semiconductor memory comprising a synchronous dynamic RAM having mask/disable terminals and operating in synchronism to an external clock (described as SDRAM hereinafter) as one example of the conventional technology will be described. FIG. 16 is a block diagram showing general configuration of a semiconductor memory based on the conventional technology. FIG. 16 especially shows a SDRAM based on the memory bank system enabling management of a memory capacity larger than the address space of a MPU by utilizing a MPU (Micro Processing Unit).

Brief Summary Text (7):
In FIG. 16, SDRAM 100 comprises memory arrays each in turn comprising memory cells as memory units in a matrix form, and the memory arrays are divided into two banks (bank 0, bank 1) with each bank further divided into a plurality of blocks. Each bank has a row decoder 102 and a column decoder 103, and one memory cell is selected from a memory array 101 by the decoders 102, 103. The row decoder 102 is a circuit that receives a row address signal 110 and selects one word line from those each identifying a memory cell in the row direction. The column decoder 103 is a circuit that receives a column address signal 111 and selects one bit line from those each identifying a memory. cell in the column direction. A sense amplifier 104 for amplifying an electric charge stored in a memory cell is connected to each bit line.

Brief Summary Text (8):
Data in a memory cell identified by the row decoder 102 and column decoder 103 according to a data read command in the bank 0 or bank 1 is inputted via a global database (GDB) into a write amplifier/sense buffer 105. In this SDRAM 100, input/output of data comprising a plurality of bits is capable, and for instance when input/output of 16-bit data is to be executed, 2-byte data for a memory cell identified according to inputted row address signal 110 as well as according to inputted column address signal 111 is latched in the write amplifier/sense buffer 105 for parallel output of data.

Brief Summary Text (13):
The RAS signal 120, CAS signal 121 and WE signal 122 inputted into the bank 0 or bank 1 are outputted from a control signal latch 113. The control signal latch 113 receives a command signal 125 from a command decoder 112, latches a control signal indicated by the command signal 125, and outputs the RAS signal 120, CAS signal 121 and WE signal 122 each as a signal level capable of expressing a control instruction according to a combination of the signals.

Brief Summary Text (14):
A command decoder 112 receives a /CS signal, a /RAS signal, a /CAS signal and a /WE signal, decides a control instruction according to a combination of these signals, and outputs a command instruction indicating the control instruction. The command decoder 112 also decides an access mode according a combination of the /CS signal, /RAS signal, /CAS signal and /WE signal, and outputs a mode signal 126 indicating the access mode.

Brief Summary Text (16):
The SDRAM 100 operates according to a synchronous signal (CLK) given from the outside such as a system clock from the MPU, and can executes operations in the internal circuit described above at a high speed. A clock buffer 115 receives a clock signal (CLK) given from the outside and a clock enable signal (CKE) controlling output of the clock signal, and supplies the received clock signal to each of the circuits described above. The clock buffer 115 also provides the received clock enable signal to each of the command decoder 112, address buffer/register & bank select 108 and I/O data buffer/register 107.

Brief Summary Text (20):
FIG. 17 is an explanatory view showing key sections of a semiconductor memory according to the conventional technology, and shows configuration of a data input/output section of the SDRAM according to the conventional technology. The I/O data buffer/register 107 shown in FIG. 16 is actually divided, as shown in FIG. 17, into an I/O data buffer 131 connected to the data input/output terminals for data signals DQ0 to DQ15 and DQM input buffers 132 and 133 connected to mask terminals for the DQML and DQMU signals respectively.

Brief Summary Text (28):
In a DRAM such as a SDRAM, generally a signal level of one data is determined by comparing signal levels of complimentary data signals each other, so that a signal level of data sent to the GDB 106 is decided by the two signals GDB0 and GDB1, and herein description is made assuming that a signal level of GDB0 against a level of a signal sent to the GDB1 is a signal level of data inputted to or outputted from the I/O data buffer 131.

Brief Summary Text (94):
Testing for checking operations of semiconductor memories including those each having a plurality of pins of data input/output terminals and also having a mask/disable terminal for selectively enabling data write and data read like the SDRAM as described above is generally carried out by using an IC tester having the terminal connection pins connected to terminals of the semiconductor memory.

Detailed Description Text (2):
Detailed description is made hereinafter for embodiments of the semiconductor memory according to the present invention with reference to the drawing. It should be noted that the present invention is not limited by the embodiments. Description of the semiconductor memory according to the present invention is made below with a reference to a SDRAM, which operates in synchronism to an external clock, as an example thereof.

Detailed Description Text (3):
FIG. 1 is an explanatory view showing connection between an IC tester and each of semiconductor memory devices 1 to 4 in testing of semiconductor memory devices each with the semiconductor memory according to the present invention incorporated therein (in this embodiment, a packaged SDRAM) with the IC tester. When testing with the IC tester, generally a plurality of semiconductor memory devices are connected to receptacles thereof to simultaneously test the semiconductor memory devices to shorten the time required for the testing.

Detailed Description Text (9):
FIG. 2 is a block diagram showing general configuration of a semiconductor memory according to Embodiment 1 of the present invention. In FIG. 2, a SDRAM 10, which is a semiconductor memory, shows a SDRAM similar to the SDRAM described a the conventional technology and based on the memory bank system in which, by using a MPU, it is possible to manage a memory capacity larger than an address space of the MPU.

Detailed Description Text (10):
The SDRAM according to the present invention is different from the conventional technology shown in FIG. 16 in that a test mode decoder 26 and a DQM switch circuit 27 are provided, and that a DQML signal and a DQMU signal inputted from the outside are given in the normal mode as they are as a MASK0 signal and a MASK1 signal to each bank, and either one of the DQML signal and DQMU signal is given in the testing mode to both of the MASK0' signal and MASK1 signal, which are supplied to each bank.

Detailed Description Text (11):
In the SDRAM 10 shown in FIG. 2, a memory array, in which memory cells are arranged in a matrix form, is divided into two banks (bank 0 and bank 1). Further, each bank is

divided to a plurality of blocks. Each block has a row decoder 12 and a column decoder 13, and selects one memory cell from a memory array 11 in each block.

Detailed Description Text (13):
For instance, in a case of 1M-bit SDRAM, each of the bank 0 and bank 1 has a memory space of 64K bytes (512K bits), and each bank is quartered to blocks each having a memory capacity of 128K bits (128K memory cell). In this case, a row decoder for each block identifies one word line from 512 row addresses, and a column decoder/sense amplifier identifies one bit line from 256 column addresses.

Detailed Description Text (14):
In the bank 0 or bank 1, data in a memory cell identified by the row decoder 12 and column decoder 13 in response to a data read command is inputted via a global data bus (GDB) 16 into the write amplifier/sense buffer 15 (it should be noted that, in this case, the sense buffer functions). Data comprising a plurality of bits can be inputted into or outputted from the SDRAM 10, and when 16-bit data is inputted or outputted, data for 2 bytes in a memory cell identified according to the inputted row address signal 20 and column address signal 21 can be latched in the write amplifier/sense buffer 15 and can be outputted in parallel.

Detailed Description Text (21):
The RAS signal 30, CAS signal 31 and WE signal 32 inputted into the bank 0 and bank 1 are outputted from a control signal latch 23. The control signal latch 23 receives a command signal 35 from a command decoder 22, latches a control command indicated by the command signal 35, generates and outputs each signal so that the latched control instruction can be expressed with a combination of the three signals of RAS signal 30, CAS signal 31 and WE signal 32.

Detailed Description Text (22):
The command decoder 22 receives a /CS signal, a /RAS signal, a /CAS signal and a /WE signal, decides a control instruction according to a combination of these signals, and outputs a command signal 35 indicated by the control instruction. The command decoder 22 decides an access mode for data according to a combination of the /CS signal, /RAS signal, /CAS signal and /WE signal, and outputs a mode signal 36 indicating the access mode. This mode signal 36 is inputted into a mode register 24.

Detailed Description Text (24):
The SDRAM 10 operates according to a synchronous signal (CLK) given from the outside such as, for instance, a system clock from a MPU, and operates at a high speed. A clock buffer receives a clock enable signal (CKE) for controlling output of a clock signal (CLK) given from the outside and the clock signal, and supplies the received clock signal to each circuit.

Detailed Description Text (25):
The clock buffer 25 provides the received clock enable signal to the command decoder 22, address buffer/register & bank select 18 and I/O data buffer/register 17, and when the circuits are not to be operated, terminates supply of the clock signal to realize reduction of power consumption.

Detailed Description Text (28):
The test instruction signal (TCS signal) 37 is an operation mode signal for testing a semiconductor memory with an IC tester, which is a signal outputted from the command decoder 22 when the semiconductor memory is set in an IC tester and the /RAS signal, /CAS signal and /WE signal each indicating the test mode are transmitted from the IC tester.

Detailed Description Text (29):
An address signal given from the address buffer/register & bank select 18 to the test mode decoder 26 specifies a type of testing to be executed actually. The test mode decoder 26 receives a test instruction signal 37 indicating a testing mode from the command decoder 22, and activates the test signal 38 when a signal specifying the write mask/read disable testing is received from the address buffer/register & bank select 18.

Detailed Description Text (33):
It should be noted that, a refresh controller for reading out data written in a memory cell into a bit line, amplifying the data signal with a sense amplifier, and rewriting the data again in the bit line, namely for refreshing is required to an actual SDRAM, but in FIG. 2 the refresh controller is omitted to simplify description concerning

operations of the SDRAM.

Detailed Description Text (34):
FIG. 3 is a view showing general configuration of a semiconductor memory device packaged therein according to Embodiment 1, and shows a state wherein the SDRAM 10 shown in FIG. 2 is packaged (described as SDRAM device hereinafter). In FIG. 3, the SDRAM comprises fifty pin terminals.

Detailed Description Text (36):
The /WE, /CAS and /RAS are terminals for receiving a control clock for the SDRAM. The /WE terminal relates to a data write/read operation, the /CAS terminal relates to latching of a column address, and /RAS terminal relates to latching of a row address. Furthermore, the /CS terminal is a chip select terminal for setting each SDRAM device in an active state when a SDRAM module is constructed with a plurality of SDRAM devices. The signals inputted from the four terminals of /WE, /CAS, /RAS and /CS are guided to the command decoder 22 shown in FIG. 2, and an operation mode of the SDRAM such as the control instruction or access mode as described above is decided according to a combination of the signal.

Detailed Description Text (37):
The CLK and CKE are terminals connected to the clock buffer 25 shown in FIG. 2, and give a synchronous clock signal (CLK) and a clock enable signal (CKE) for the CLK respectively. The DQML and DQMU are mask/disable terminals, and are connected to the I/O data buffer/register 17 shown in FIG. 2. In the SDRAM device shown in FIG. 3, the DQML terminal controls mask/disable of the data input/output terminals DQ0 to DQ7, while the DQMU terminal controls mask/disable of the data input/output terminals DQ13 to DQ15.

Detailed Description Text (38):
FIG. 4 is a view showing detail configuration of the I/O data buffer/register 17, DQM switch circuit 27 and write amplifier/sense buffer 15 in the semiconductor memory according to Embodiment 1 of the present invention. FIG. 4 shows configuration comprising a write amplifier & sense buffers 51 and an I/O data buffers 41 corresponding to the write sense amplifier & sense buffers 141 and I/O data buffers 131 shown in FIG. 18 to FIG. 22 respectively. Detail description is made below for operations for data input and output by the SDRAM 10 and operation of the DQM switch circuit 27 with reference to FIG. 4.

Detailed Description Text (56):
Next, description is made for a semiconductor memory according to Embodiment 2 of the present invention. Embodiment 2 is different from Embodiment 1 in that the test signal 38 and test instruction signal 39 are supplied from the test mode decoder 26 to a DQM switch circuit 90, and that configuration of the DQM switch circuit 90 has been modified according to the change above. FIG. 7 is a block diagram showing general configuration of the semiconductor memory according to Embodiment 2. In the SDRAM 40 shown in FIG. 7, which is a semiconductor memory according to Embodiment 2, the test mode decoder 26 generates a test signal 38 and a test instruction signal (TCS signal) 39 according to a test instruction signal (TCS signal) inputted from the command decoder 22 as well as according to a portion of address signals outputted from the address buffer/register & bank select 18, while the DQM switch circuit 90 receives the test signal 38 and test instruction signal 39.

Detailed Description Text (57):
FIG. 8 is an explanatory view showing key sections of the semiconductor memory according to the present invention, more specifically configuration of a data input/output section and a SQM switch circuit 90 in the SDRAM 40. FIG. 8 shows configuration comprising write amplifier & sense buffers 54 and an I/O data buffers 44 corresponding to the write amplifier & sense buffers 141 and I/O data buffers 131 shown in FIG. 18 to FIG. 22. In FIG. 8, data signals inputted to the data input/output terminals DQ0 to DQ15 are inputted to the I/O data buffers 44 corresponding to the data input/output terminals respectively, and a DQML signal and DQMU signal inputted to the DQML terminal and a DQMU terminal respectively are inputted to a DQM input buffer 45 and a DQM input buffer 46 corresponding to the DQML terminal and DQMU terminal respectively.

Detailed Description Text (80):
Next, description is made for a semiconductor memory according to Embodiment 3 of the present invention. Embodiment 3 is different from Embodiment 2 described above in that the test signal 38 and two test instruction signals 67, 68 are supplied from the test

mode decoder 26 to a DQM switch circuit, and that, when the test instruction signal 67 indicates "H" level, the DQML signal is supplied as the MASK0' signal or MASK1 signal, and when the test instruction signal 68 indicates a "H" level, the DQML signal is supplied as the MASK0' signal or MASK1' signal, namely that a mask/disable terminal (DQML or DQMU) to be used in testing can be selected according to the test instruction signals 67, 68. FIG. 12 is a block diagram showing general configuration of the semiconductor memory according to Embodiment 3. In the SDRAM 50 shown in shown in FIG. 12, which is the semiconductor memory according to Embodiment 3, the two test instruction signals (TCS1 signal, TCS2 signal) are outputted, and the test decoder 26 receives the TCS1 signal 65 and TCS2 signal 66 as well as a portion of addresses of the address buffer/register & bank select 18, and outputs the test signal 38 as well as the TCS1 signal and TCS2 signal (described as TCS1 signal 67 and TCS signal 68 hereinafter), and these three signals are inputted to a DQM switch circuit 91. It should be noted that, when either one of the TSC1 signal 65 and TCS2 signal 66 indicates a "H" level, the test signal 38 indicates a "H" level and is outputted from the test mode decoder 26. Which one of the TCS1 signal 67 and TCS2 signal 68 should be set in a "H" level may be switched according to an address signal inputted into the test mode decoder 26 in place of outputting the TCS1 signal 65 and TCS2 signal from the command decoder 22.

Detailed Description Text (81):
FIG. 13 is an explanatory view showing configuration of the key sections of the semiconductor memory according to Embodiment 3, and shows detail configuration of a data input/output section and the DQM switch circuit 91 in the SDRAM 50. FIG. 13 especially shows write amplifier & sense buffers 57 and I/O data buffers 47 corresponding to the write amplifier & sense buffers 141 and I/O data buffers 131 shown in FIG. 18 to FIG. 22 respectively. In FIG. 13, each data signal inputted to each of the data input/output terminals DQ0 to DQ15 is inputted to the I/O data buffer 47 in each respective data input/output terminal, while the DQML signal and DQMU signal inputted to the DQML terminal and DQMU terminal respectively are inputted to the DQML buffer 48 and DQM input buffer 49 corresponding to the DQML terminal and DQMU terminal respectively.

Detailed Description Text (100):
Further, description of Embodiments 1 to 3 assumed a SDRAM as a basic component of a semiconductor memory, but such devices as an ordinary DRAM, or SRAM, or EPROM, or EEPROM may be used as a basic component, and any specific type of memory device is not required on the condition that the memory has a plurality of mask/disable terminals.

Other Reference Publication (2):
Alves et al., "Testing Embedded Single and Multi-port RAMs using bist and Boundary Scan", (c) 1992 IEEE, p. 159-163.

WEST

Generate Collection Print

L25: Entry 84 of 101 File: USPT Mar 16, 1999

DOCUMENT-IDENTIFIER: US 5883855 A
TITLE: High speed semiconductor memory with burst mode

Detailed Description Text (6):
The command decoder (CDEC) 102 takes-in external command signals /RAS (RAS (Row Address Strobe) bar), /CAS (CAS bar), /WE (Write Enable bar), and /CS (Chip Select bar) at the clock edges of the internal reference clock signals ICLK, decodes the commands that are given in combination with these signals from the outside, and generates internal signals corresponding to the respective commands. In the synchronous DRAM, although there are several kinds of commands such as activation commands, FIG. 3 shows only the RW signals which correspond to read/write commands and the MDRS signals which correspond to mode register set commands as those signals that are relevant to the invention.

Detailed Description Text (73):
The command decoder (CDEC) 102 takes-in external command signals /RAS, /CAS, /WE, and /CS at the clock edges of the internal reference clock signals ICLK, decodes the commands that are given in combination with these signals from the outside, and generates internal signals corresponding to the respective commands. In the synchronous DRAM, although there are several kinds of commands such as activation commands, FIG. 8 shows only the RW signals which correspond to read/write commands and the MDRS signals which correspond to mode register set commands as those signals that are relevant to the invention.

L25: Entry 85 of 101 File: USPT Mar 9, 1999

DOCUMENT-IDENTIFIER: US 5880998 A
TITLE: Synchronous semiconductor memory device in which current consumed by input buffer circuit is reduced

Brief Summary Text (17):
The SDRAM further includes an external signal input buffer circuit 6 for taking in and latching external signals ZCS, ZRAS, ZCAS and ZWE in synchronization with the rise of internal clock signal intCLK for generating an internal control signal; a command decoder 8 for generating a signal designating an operation mode designated in accordance with the internal control signal from external signal input buffer 6; and an internal control signal generating circuit 10 for generating a necessary internal control signal in accordance with an internal operation mode designating signal from command decoder 8. Internal control signal generating circuit 10 also operates in synchronization with internal clock signal intCLK and activate/inactivate various internal control signals in accordance with the internal clock signal intCLK.

Detailed Description Text (21):
FIG. 4 shows a structure of a main portion of an SDRAM in accordance with a first embodiment of the present invention. In FIG. 4, portions corresponding to those of FIG. 1 are denoted by the same reference characters and detailed description thereof is not repeated. In the structure shown in FIG. 4, to the gate of p channel MOS transistor PQ3 for shutting off a current path of input buffer circuit 30 receiving external signal EXT, an output signal intZCKE0 from the first latch circuit 2b is applied as an input buffer enable signal. The internal clock enable signal intZCKE from the second latch circuit 2c is applied to internal clock generating circuit 4, to control validity/invalidity of the internal clock signal intCLK. An output signal from input buffer circuit 30 is applied to a latch circuit 35 which is set to a latch state in response to internal clock signal intCLK from internal clock generating circuit 4. Latch circuit 35 takes in a signal applied from input buffer circuit 30 in accordance with the rise of internal clock signal intCLK, and it latches the signal while the internal clock signal intCLK is at the L level. An internal signal intCOM from latch circuit 35 is any of an internal control signal (corresponding to external control signals generating a command), an address signal bit or an internal write data, which is applied to command decoder, address decoder or write circuit, respectively (see FIG. 15).

WEST

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L25: Entry 89 of 101 File: USPT Sep 8, 1998

DOCUMENT-IDENTIFIER: US 5805504 A
TITLE: Synchronous semiconductor memory having a burst transfer mode with a plurality of subarrays accessible in parallel via an input buffer

Detailed Description Text (5):
A command decoder (CDEC) 22 fetches various external command signals such as a row address strobe signal RAS, a column address strobe signal CAS, a write enable signal WE and a chip select signal CS, in response to a leading or rising edge of the internal reference clock ICLK, and decodes the command designated by a combination of the various external command signals, to generate various internal control signals. In the synchronous DRAM, the commands includes several different commands such as an activation command, however, for simplification of drawing and description, only an internal read/write signal RW corresponding to a read/write command and relating to the present invention is shown.